Introduction

A long time ago, before integrated microprocessors, there was a wonderful chip with a number designation of 74181 (a 4-bit ALU). This was a time when you made up a microprocessor using many TTL logic chips. Two or four of these ALU chips made the core of a microprocessor. For a 16-bit ALU, there was a companion chip designated 74182 which was used to speed up the carry output.

These chips are no longer readily available but the published circuit diagram makes it useful for simulation (see datasheets included in this package).

Purpose

Many students in Electrical Engineering learn how to use and program a microprocessor but very few know what goes on inside. This article will give the reader insight into the inner workings of a very simple microprocessor that can be extended to more powerful designs. I will use a visual method of ANDs ORs and Inverters to implement the data paths and controls. In order to do that, we have to use a logic simulator to test the design. Fortunately, there is a simple free program (CEDAR Logic) that accomplishes this task and is easy to learn.
You can download it from the following URL:
http://sourceforge.net/projects/cedarlogic/?source=dlp

Design Description

The file BlockDiagram.pdf shows the data paths that feed the ALU and RAM. There is only 1 Accumulator for simplicity. Control logic is centered on a 32-bit ROM that implements the sequences for fetching data from RAM and decoding the instructions. You can view the sequences as a state diagram but traditionally it's called horizontal programming (see PicoCode.pdf). Each program word is 32 bits wide and includes the next address of the flow. Two way branching is possible on the Carry Latch, Zero Latch and bit 0 of the Op Code Register. A 16 way branch can be performed on the high-order 4 bits of the Op Code Register.
As mentioned before, the Arithmetic-Logic-Unit is based on the 74181 datasheet. Refer to ALU.jpg for an image of the circuit as presented by the simulator. The page illustrated by A-SidePath.jpg shows the data paths feeding the A-side of the ALU.

SystemRAM.jpg shows the B-side data path for the ALU. Sequence.jpg and ClockAndDisplay.jpg complete the entire design.

Instruction Set

The instructions that this microprocessor executes from RAM consists of 16 op codes as follows:

Mnemonic	Op Code	Operand	Addressing Mode	ZL	CL
NOP	00	-----	Inherent	--	--
LDA	10	Data	Immediate	↕	--
LDA	11	Data Addr	Direct	↕	--
BRA	20	Branch Addr	Direct	--	--
ADD	30	Data	Immediate	↕	↕
ADD	31	Data Addr	Direct	↕	↕
STA	40	Data Addr	Direct	↕	--
ADC	50	Data	Immediate	↕	↕
ADC	51	Data Addr	Direct	↕	↕
BRZ	60	Branch Addr	Direct	--	--
SUB	70	Data	Immediate	↕	↕
SUB	71	Data Addr	Direct	↕	↕
BCS	80	Branch Addr	Direct	--	--
SBC	90	Data	Immediate	↕	↕
SBC	91	Data Addr	Direct	↕	↕
INC	A0	-----	Inherent	↕	--
DEC	B0	-----	Inherent	↕	--
AND	C0	Data	Immediate	↕	--
AND	C1	Data Addr	Direct	↕	--
ORA	D0	Data	Immediate	↕	--
ORA	D1	Data Addr	Direct	↕	--
EOR	E0	Data	Immediate	↕	--
EOR	E1	Data Addr	Direct	↕	--
CLC	F0	-----	Inherent	--	0
SEC	F1	-----	Inherent	--	1

ALU FUNCTIONS

HEX	S3	S2	S1	S0	M=H	M=L, Ci=H	M=L, Ci=L
0	L	L	L	L	\A	A	A plus 1
1	L	L	L	H	\A or \B	A or B	
2	L	L	H	L	\A and B	A or \B	
3	L	L	H	H	Logic 0	Minus 1	
4	L	H	L	L	\(A and B)	A plus (A and \B)	
5	L	H	L	H	\B	(A or B) plus (A and \B)	
6	L	H	H	L	A xor B	A minus B minus 1	A minus B
7	L	H	H	H	A and \B	(A and B) minus 1	
8	H	L	L	L	\A or B	A plus (A and B)	
9	H	L	L	H	\A xor \B	A plus B	A plus B plus 1
A	H	L	H	L	B	(A or \B) plus (A and B)	
B	H	L	H	H	A and B	(A and B) minus 1	
C	H	H	L	L	Logic 1	A plus A	
D	H	H	L	H	A or \B	(A or B) plus A	
E	H	H	H	L	A or B	(A or \B) plus A	
F	H	H	H	H	A	A minus 1	

Notes:

1. This table uses active high inputs on the A-side and B-side . The Carry In and Carry Out signals negative logic.
2. Operations in red are most useful.

CONTROLS

V	Spare	
U	Spare	
T	Spare	
S	CCR Gate	0 – select Co and Z, 1 – select ALU0 and ALU1
R	B Mux Sel	0 – select RAM data, 1 – select CCR
Q	En ZL Clk	1 – Enable Zero Latch Clock
P	En CL Clk	1 – Enable Carry Latch Clock
O	Sel ALU Src	0 – select IC, 1 – select ALU
M N	Ci Src	0X – Low, 10 – High, 11 – CL
L	En RAM Wrt	1 – Enable RAM Write Clock
K	En Inst Clk	1 – Enable Op Code Register Clock
J	En MAR Clk	1 – Enable Memory Address Register Clock
I	A Mux Sel	0 – select IC, 1 – select Accumulator
H	En IC Clk	1 – Enable Instruction Counter Clock
G	En Acc Clk	1 – Enable Accumulator Clock
E	Mode	0 – Arithmetic, 1 – Logic
D	S3	See chart above
C	S2	“
B	S1	“
A	S0	“